



IN THE CLAIMS

1-20. (Cancelled)

21. (Currently Amended) A ferroelectric memory device comprising:
a first interlayer insulating layer formed on a semiconductor substrate;
a buried contact structure ~~connected to~~ contacting the substrate through a first contact hole extending through the first interlayer insulating layer, the buried contact structure formed ~~on~~ over and in contact with the first interlayer insulating layer;
a blocking layer formed ~~on~~ over and in contact with the buried contact structure and the first interlayer insulating layer;
a second interlayer insulating layer formed on the blocking layer; and
a ferroelectric capacitor with a metallic lower electrode, wherein the lower electrode that fills a second contact hole and connects to contacts the buried contact structure through the a second contact hole that penetrates the second interlayer insulating layer and the blocking layer, and wherein the ~~ferroelectric capacitor being~~ lower electrode is formed ~~on~~ over and in contact with the second interlayer insulating layer.

22. (Previously presented) The ferroelectric memory device according to claim 21, wherein the blocking layer comprises a material chosen from the group consisting of silicon oxynitride (SiON), silicon nitride (SiN), and aluminum oxide.

23. (Original) The ferroelectric memory device according to claim 21, wherein a diameter of the second contact hole is larger than a diameter of the first contact hole.

24. (Original) The ferroelectric memory device according to claim 21, wherein the buried contact structure is made of tungsten (W).

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